

Neil Adit

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Education

Cornell University

PHD IN COMPUTER ENGINEERING

- Research Interests: Compilers, Computer architecture, Machine Learning, Cloud computing
- Committee: Adrian Sampson (chair), Zhiru Zhang, Chris De Sa
- Courses: Advanced ML Systems, Computer Vision, Advanced Compilers, Datacenter Computing, Parallel Computing

Aug. 2018 - Present

GPA: 4/4

Indian Institute of Technology, Bombay

B.TECH + M.TECH IN ELECTRICAL ENGINEERING

- Masters in Microelectronics, Minor in Computer Science
- Advisor: Sachin Patkar

July 2013 - June 2018

GPA: 9.05/10

Publications

Dense Pruning of Pointwise Convolutions in the Frequency Domain

Mark Buckler, [Neil Adit](#), Yuwei Hu, Zhiru Zhang, and Adrian Sampson

arxiv preprint 2021

Software-Defined Vector Processing on Manycore Fabrics

Philip Bedoukian, [Neil Adit](#), Edwin Peguero, Adrian Sampson

MICRO 2021

Dagger: Efficient and Fast RPCs in Cloud Microservices with Near-Memory Reconfigurable NICs

Nikita Lazarev, Shaojie Xiang, [Neil Adit](#), Zhiru Zhang, Christina Delimitrou

ASPLOS 2021

Dagger: Towards Efficient RPCs in Cloud Microservices with Near-Memory Reconfigurable NICs

Nikita Lazarev, [Neil Adit](#), Shaojie Xiang, Zhiru Zhang, and Christina Delimitrou

IEEE CAL 2020

Industry Experience

Microsoft Research

RESEARCH INTERN | GUIDE: OFER DEKEL

- Developed algorithms to accelerate sparse ML models on commodity hardware in the Machine Learning and Optimization group, MSR
- Demonstrated wall-clock speedups on sparse kernel execution using the ONNX runtime library backend

Redmond, WA, USA

May 2021 - Aug 2021

Intel Labs

GRADUATE RESEARCH INTERN | GUIDE: FABRIZIO PETRINI

- Designed and implemented high performance computing algorithms for sparse computations on Intel's breakthrough research architecture

Santa Clara, CA, USA

May 2019 - Aug 2019

SIEMENS Research

SUMMER INTERN | GUIDE: DR. AMIT KALE AND PRABHU TEJA

- Designed and demonstrated Kidney segmentation in CT images for clinical diagnosis using Laplacian Mesh Deformation
- Generated a deformable Kidney model from annotated dataset using Coherent Point Drift and Procrustes analysis in MATLAB
- Applied Random Forest training to a spectral clustered part of Kidney using HOG feature to enhance boundary detection
- Achieved Dice Coefficient of 0.85 showing precision of segmentation, on incorporating Active Shape Models (ASM)

Bangalore, India

May 2016 - Jul. 2016

Research Experience

Software-Defined Vectors on Manycore

GUIDE: PROF. ADRIAN SAMPSON, CORNELL UNIVERSITY

- Worked with Philip Bedoukian on vector programming model that allows dynamic reconfiguration of manycore tiles into vector engines
- Modeled memory access synchronization on scratchpad between decoupled vector cores in gem5
- Implemented optimized versions of Polybench benchmark kernels for manycore and vector architecture

Ithaca, NY, USA

Jan. 2019 - Aug. 2020

Frequency Domain Pruning of Pointwise Convolutions

GUIDE: PROF. ADRIAN SAMPSON, CORNELL UNIVERSITY

- Worked with Mark Buckler on exploiting spatial redundancy in depthwise convolutions by pruning in the frequency domain
- Developed a novel training method for learning dense pruning while maintaining task accuracy, showing speedup on efficient networks like MobileNetV2

Ithaca, NY, USA

Aug. 2018 - Sep. 2021

Near-Memory Reconfigurable NICs

Ithaca, NY, USA

GUIDE: PROF. CHRISTINA DELIMITROU, CORNELL UNIVERSITY

Jan. 2020 - Aug. 2020

- We offload the RPC stack on a FPGA which is tightly coupled with the host CPU via memory interconnects, Intel UPI in this case
- Implemented communication schemes between host applications and NIC
- Designed queue management for asynchronously sending packets in a single connection
- The initial work was accepted at **IEEE CAL** and the extended work at **ASPLOS 2021**

Accelerating 1x1 Convolutions using Systolic Arrays

Ithaca, NY, USA

GUIDE: PROF. ZHIRU ZHANG, CORNELL UNIVERSITY

Oct. 2018 - Dec. 2018

- Implemented pointwise convolutions in MobileNets on Zynq ZC-706 using systolic arrays.
- Optimized streaming of input activations using quantization, bit packing and padding.
- Designed an efficient Dataflow architecture to minimize overhead read/write computations.
- Achieved close to ideal, 215x speedup using 16x16 parallel PEs for systolic array architecture.

Parallel Sparse Matrix Solution on FPGA

Mumbai, India

GUIDE: PROF. SACHIN PATKAR, IIT BOMBAY

Jul. 2017 - Jun. 2018

- Accelerating sparse matrix solvers for performance improvements in SPICE circuit simulators
- Designing a stack based processor with pipelined FPU to process LU expressions parallelly
- Implemented Gilbert-Peierls LU decomposition on ZedBoard using SDSoC and Vivado HLS
- Achieved upto 6x speedup using parallel hardware directives, optimizing off-chip memory access and minimizing arithmetic operations

Person Re-Identification using Deep Learning

Mumbai, India

GUIDE: PROF. SUBHASIS CHAUDHURI, IIT BOMBAY

Jul. 2017 - Dec. 2017

- Developing a Deep Learning model to spot person of interest across cameras for surveillance applications
- Modelled a RNN (temporal features) and CNN (spatial features) based Siamese network for video-based re-identification in Torch
- Applied trained pose detection model to fine-tune model parameters to conduct pose based matching
- Achieved rank-1 accuracy 60% comparable to state-of-the-art with smaller test image sequence on iLIDS-VID dataset

Academic Achievements

2018	Eastman Fellowship , Cornell University	Ithaca, U.S.A
2017	Excellence in Teaching Assistantship , EE, IIT Bombay	Mumbai, India
2013	All India Rank 242 , IIT Joint Entrance Exam (JEE)-Advanced, among 1.4 million examinees	India
2012	Ranked 115 , KVPY Scholarship, Govt. of India , among 200,000 candidates	India
2012	Top 1% , National Physics Olympiad	Delhi, India
2011	Ranked 20 , Regional Mathematics Olympiad (RMO) and among top 900 nationally to compete in Indian National Mathematical Olympiad (INMO)	Delhi, India

Extracurricular Activity

Institute Student Mentorship Programme (ISMP)

IIT Bombay, India

STUDENT MENTOR

Aug. 2016 - May. 2018

Selected for 2 consecutive years as part of team of 82 mentors from 368 applicant.

- Mentored 24 students for smooth transition to campus life, supporting their academic & co-curricular endeavors

Formula Student Racing Team

IIT Bombay, India

DESIGN ENGINEER

Sep. 2014 - Apr. 2016

A team of 70 students building India's fastest electric racecar for Formula Student UK, an international race car design competition. Won FS Award for 2 consecutive years worth £3000 (2 out of 48 non-UK teams) for major design improvements

- Headed a team of 5 Engineers to design onboard data logging and real-time remote wireless data monitoring GUI system
- Implemented team's first CAN protocol to improve reliability in communication and reduce wiring harness
- Implemented Electronic Differential and Regenerative Braking for the first time within the team
- Achieved 2x reduction in size and weight of PCB enclosure by optimized routing in boards